1 The _____ format is usually used to store data)
a) BCD
b) Decimal
c) Hexadecimal
d) Octal

2 The 8-bit encoding format used to store data in a computer is _____
a) ASCII
b) EBCDIC
c) ANCI
d) USCII

3 A source program is usually in _____
a) Assembly language
b) Machine level language
c) High-level language
d) Natural language

4 Which memory device is generally made of semiconductors?
a) RAM
b) Hard-disk
c) Floppy disk
d) Cd disk

5 The small extremely fast, RAM's are called as _____
a) Cache
b) Heaps
c) Accumulators
d) Stacks

6 The ALU makes use of _____ to store the intermediate results.
a) Accumulators
b) Registers
c) Heap
d) Stack

7 The control unit controls other units by generating _____
a) Control signals
b) Timing signals
c) Transfer signals
d) Command Signals

8 _____ are numbers and encoded characters, generally used as operands.
a) Input
b) Data
c) Information

d) Stored Values

9 _____ bus structure is usually used to connect I/O devices.
a) Single bus
b) Multiple bus
c) Star bus
d) Rambus

10 The I/O interface required to connect the I/O device to the bus consists of _____
a) Address decoder and registers
b) Control circuits
c) Address decoder, registers and Control circuits
d) Only Control circuits

11 To reduce the memory access time we generally make use of _____
a) Heaps
b) Higher capacity RAM's
c) SDRAM's
d) Cache's

12 _____ is generally used to increase the apparent size of physical memory.
a) Secondary memory
b) Virtual memory
c) Hard-disk
d) Disks

13 The time delay between two successive initiations of memory operation _____
a) Memory access time
b) Memory search time
c) Memory cycle time
d) Instruction delay

14 The decoded instruction is stored in _____
a) IR
b) PC
c) Registers
d) MDR

15 Which registers can interact with the secondary storage?
a) MAR
b) PC
c) IR
d) R0

16 During the execution of a program which gets initialized first?
a) MDR
b) IR
c) PC

d) MAR

17 Which of the register/s of the processor is/are connected to Memory Bus?
a) PC
b) MAR
c) IR
d) Both PC and MAR

18 ISP stands for _____
a) Instruction Set Processor
b) Information Standard Processing
c) Interchange Standard Protocol
d) Interrupt Service Procedure

19 The internal components of the processor are connected by _____
a) Processor intra-connectivity circuitry
b) Processor bus
c) Memory bus
d) Rambus

20 _____ is used to choose between incrementing the PC or performing ALU operations.
a) Conditional codes
b) Multiplexer
c) Control unit
d) None of the mentioned

21 The registers, ALU and the interconnection between them are collectively called as _____
a) process route
b) information trail
c) information path
d) data path

22 To extend the connectivity of the processor bus we use _____
a) PCI bus
b) SCSI bus
c) Controllers
d) Multiple bus

23 The bus used to connect the monitor to the CPU is _____
a) PCI bus
b) SCSI bus
c) Memory bus
d) Rambus

24 _____ register Connected to the Processor bus is a single-way transfer capable.
a) PC

b) IR
c) Temp
d) Z

25 The main advantage of multiple bus organisation over a single bus is _____
a) Reduction in the number of cycles for execution
b) Increase in size of the registers
c) Better Connectivity
d) None of the mentioned

26 During the execution of the instructions, a copy of the instructions is placed in the _____
a) Register
b) RAM
c) System heap
d) Cache

27 A processor performing fetch or decoding of different instruction during the execution of another instruction is called _____
a) Super-scaling
b) Pipe-lining
c) Parallel Computation
d) None of the mentioned

28 An optimizing Compiler does _____
a) Better compilation of the given piece of code
b) Takes advantage of the type of processor and reduces its process time
c) Does better memory management
d) None of the mentioned

29 The ultimate goal of a compiler is to _____
a) Reduce the clock cycles for a programming task
b) Reduce the size of the object code
c) Be versatile
d) Be able to detect even the smallest of errors

30 In memory-mapped I/O _____
a) The I/O devices and the memory share the same address space
b) The I/O devices have a separate address space
c) The memory and I/O devices have an associated address space
d) A part of the memory is specifically set aside for the I/O operation

31 The usual BUS structure used to connect the I/O devices is _____
a) Star BUS structure
b) Multiple BUS structure
c) Single BUS structure
d) Node to Node BUS structure

32 The advantage of I/O mapped devices to memory mapped is _____
a) The former offers faster transfer of data
b) The devices connected using I/O mapping have a bigger buffer space
c) The devices have to deal with fewer address lines
d) No advantage as such

33 The system is notified of a read or write operation by _____
a) Appending an extra bit of the address
b) Enabling the read or write bits of the devices
c) Raising an appropriate interrupt signal
d) Sending a special signal along the BUS

34 The method of accessing the I/O devices by repeatedly checking the status flags is _____
a) Program-controlled I/O
b) Memory-mapped I/O
c) I/O mapped
d) None of the mentioned

35 The method of synchronising the processor with the I/O device in which the device sends a signal when it is ready is?
a) Exceptions
b) Signal handling
c) Interrupts
d) DMA

36 The method which offers higher speeds of I/O transfers is _____
a) Interrupts
b) Memory mapping
c) Program-controlled I/O
d) DMA

37 _____ is used as an intermediate to extend the processor BUS.
a) Bridge
b) Router
c) Connector
d) Gateway

38 The DMA differs from the interrupt mode by _____
a) The involvement of the processor for the operation
b) The method of accessing the I/O devices
c) The amount of data transfer possible
d) None of the mentioned

39 The DMA transfers are performed by a control circuit called as _____
a) Device interface
b) DMA controller

c) Data controller
d) Overlooker

40 In DMA transfers, the required signals and addresses are given by the _____
a) Processor
b) Device drivers
c) DMA controllers
d) The program itself

41 After the completion of the DMA transfer, the processor is notified by _____
a) Acknowledge signal
b) Interrupt signal
c) WMFC signal
d) None of the mentioned

42 The DMA controller has _____ registers.
a) 4
b) 2
c) 3
d) 1

43 Can a single DMA controller perform operations on two different disks simultaneously?
a) True
b) False

44 When the process requests for a DMA transfer?
a) Then the process is temporarily suspended
b) The process continues execution
c) Another process gets executed
d) process is temporarily suspended & Another process gets executed

45 The DMA transfer is initiated by _____
a) Processor
b) The process being executed
c) I/O devices
d) OS

46 The standard SRAM chips are costly as _____
a) They use highly advanced micro-electronic devices
b) They house 6 transistor per chip
c) They require specially designed PCB's
d) None of the mentioned

47 The drawback of building a large memory with DRAM is _____
a) The large cost factors
b) The inefficient memory organisation
c) The Slow speed of operation

d) All of the mentioned

48 To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.
a) True
b) False

49 The fastest data access is provided using _____
a) Caches
b) DRAM's
c) SRAM's
d) Registers

50 The memory which is used to store the copy of data or instructions stored in larger memories, inside the CPU is called _____
a) Level 1 cache
b) Level 2 cache
c) Registers
d) TLB

51 The larger memory placed between the primary cache and the memory is called _____
a) Level 1 cache
b) Level 2 cache
c) EEPROM
d) TLB

52 The next level of memory hierarchy after the L2 cache is _____
a) Secondary storage
b) TLB
c) Main memory
d) Register

53 The last on the hierarchy scale of memory devices is _____
a) Main memory
b) Secondary memory
c) TLB
d) Flash drives

54 In the memory hierarchy, as the speed of operation increases the memory size also increases.
a) True
b) False

55 If we use the flash drives instead of the hard disks, then the secondary storage can go above primary memory in the hierarchy.
a) True
b) False

56 The interrupt-request line is a part of the _____
a) Data line
b) Control line
c) Address line
d) None of the mentioned

57 The return address from the interrupt-service routine is stored on the _____
a) System heap
b) Processor register
c) Processor stack
d) Memory

58 The signal sent to the device from the processor to the device after receiving an interrupt is _____
a) Interrupt-acknowledge
b) Return signal
c) Service signal
d) Permission signal

59 The time between the receiver of an interrupt and its service is _____
a) Interrupt delay
b) Interrupt latency
c) Cycle time
d) Switching time

60 Interrupts form an important part of _____ systems.
a) Batch processing
b) Multitasking
c) Real-time processing
d) Multi-user

61 A single Interrupt line can be used to service n different devices.
a) True
b) False

62 Which of the following is true with respect to EEPROM?
a) contents can be erased byte wise only.
b) contents of full memory can be erased together.
c) contents can be erased using ultra violet rays
d) contents can not be erased

63 Which of the following statement is true?
a) The group of machine cycle is called a state.
b) A machine cycle consists of one or more instruction cycle.
c) An instruction cycle is made up of machine cycles and a machine cycle is made up of number of states.
d) None of the above

64 SDRAM refers to
a) static DRAM
b) synchronous DRAM
c) sequential DRAM
d) semi DRAM

65 In a DMA write operation the data is transferred
a) from I/O to memory.
b) from memory to I/O.
c) from memory to memory.
d) from I/O to I/O.

66 A Process Control Block(PCB) does not contain which of the following?
a) Code
b) Stack
c) Bootstrap program
d) Data

67 The number of processes completed per unit time is known as _____
a) Output
b) Throughput
c) Efficiency
d) Capacity

68 Which of the following is not the state of a process?
a) New
b) Old
c) Waiting
d) Running

69 The entry of all the PCBs of the current processes is in _____
a) Process Register
b) Program Counter
c) Process Table
d) Process Unit

70 A single thread of control allows the process to perform _____
a) only one task at a time
b) multiple tasks at a time
c) only two tasks at a time
d) all of the mentioned

71 Which module gives control of the CPU to the process selected by the short-term scheduler?
a) dispatcher
b) interrupt
c) scheduler

d) none of the mentioned

72 The processes that are residing in main memory and are ready and waiting to execute are kept on a list called _____
a) job queue
b) ready queue
c) execution queue
d) process queue

73 Which scheduling algorithm allocates the CPU first to the process that requests the CPU first?
a) first-come, first-served scheduling
b) shortest job scheduling
c) priority scheduling
d) none of the mentioned

74 Which algorithm is defined in Time quantum?
a) shortest job scheduling algorithm
b) round robin scheduling algorithm
c) priority scheduling algorithm
d) multilevel queue scheduling algorithm

75 Process are classified into different groups in _____
a) shortest job scheduling algorithm
b) round robin scheduling algorithm
c) priority scheduling algorithm
d) multilevel queue scheduling algorithm

76 _____ keys are present on the top row of the keyboard)
a) Function
b) Type writer
c) Numeric
d) Navigation

77 The device primarily used to provide hardcopy is the
a) CRT
b) Computer Console
c) Printer
d) Card Reader

78 Which among the device that converts computer output into a form that can be transmitted over a telephone line?
a) Teleport
b) Multiplexer
c) Concentrator
d) Modem

79 These devices provide a means of communication between a computer and outer world)
a) I/O
b) Storage
c) Compact
d) Drivers

80 The I/O devices are sometimes called the peripheral devices because they surround the CPU and memory of the computer system.
a) True
b) False